

FIG. 1
(PRIOR ART)

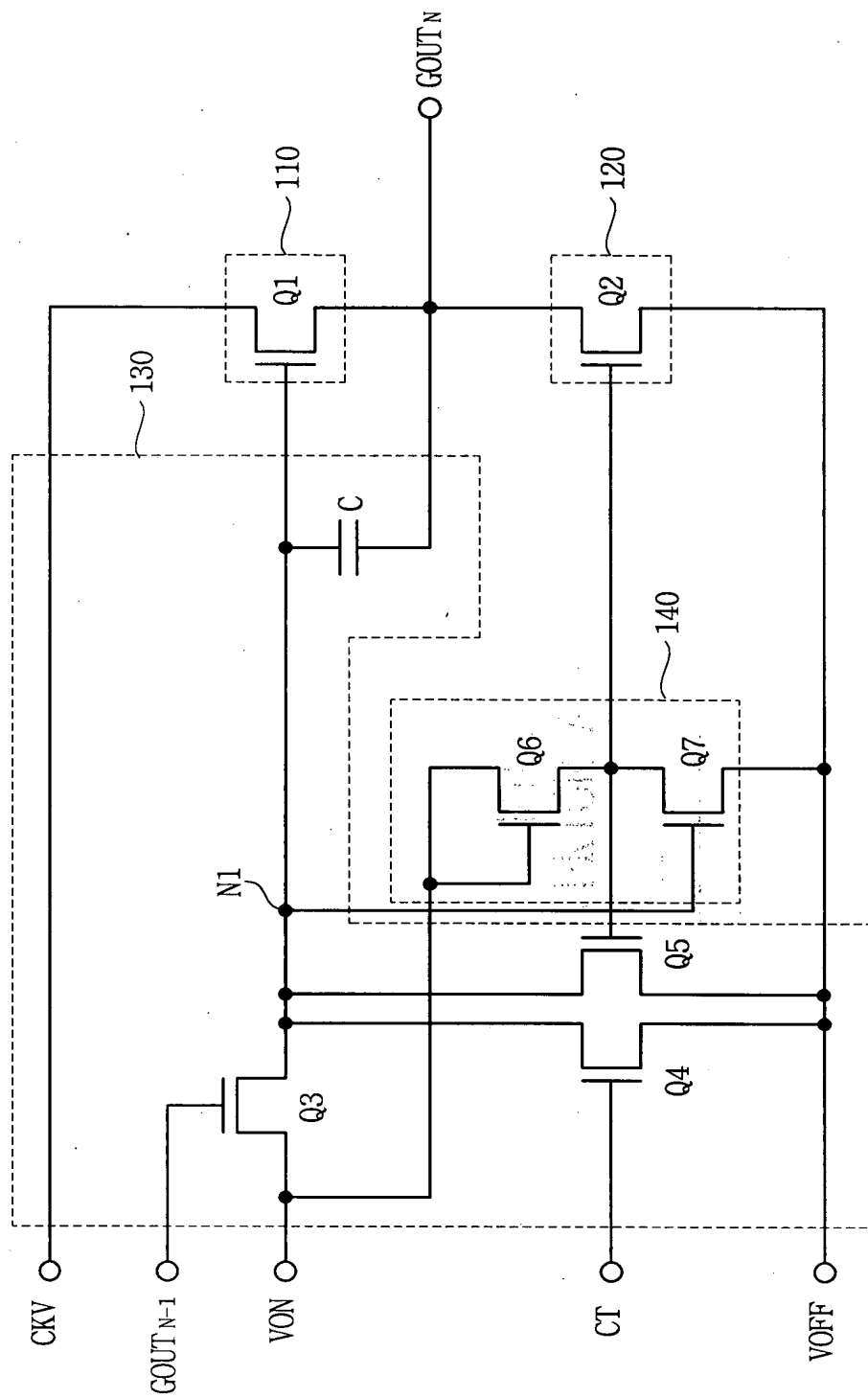


FIG. 2
(PRIOR ART)

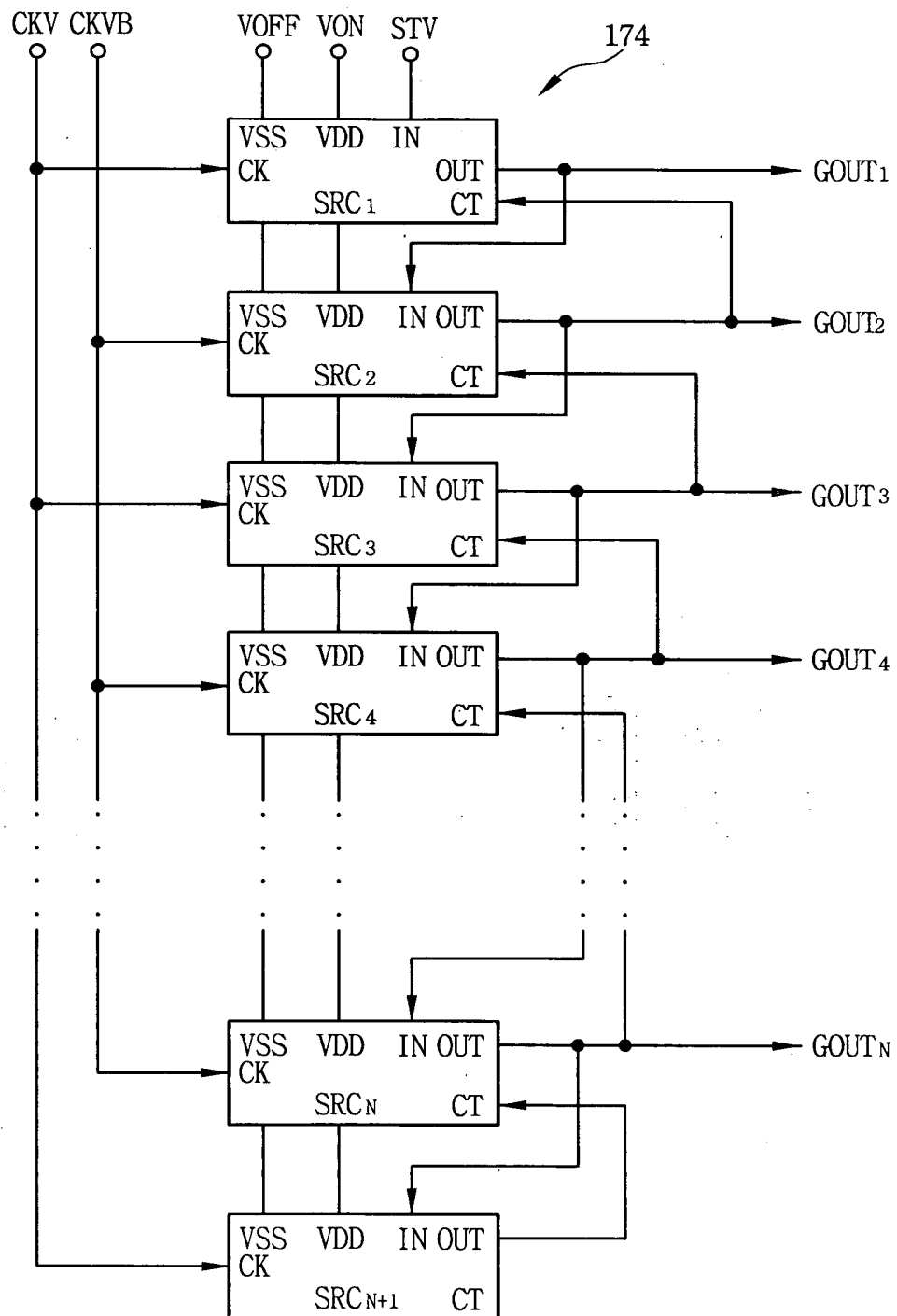


FIG. 3A
(PRIOR ART)

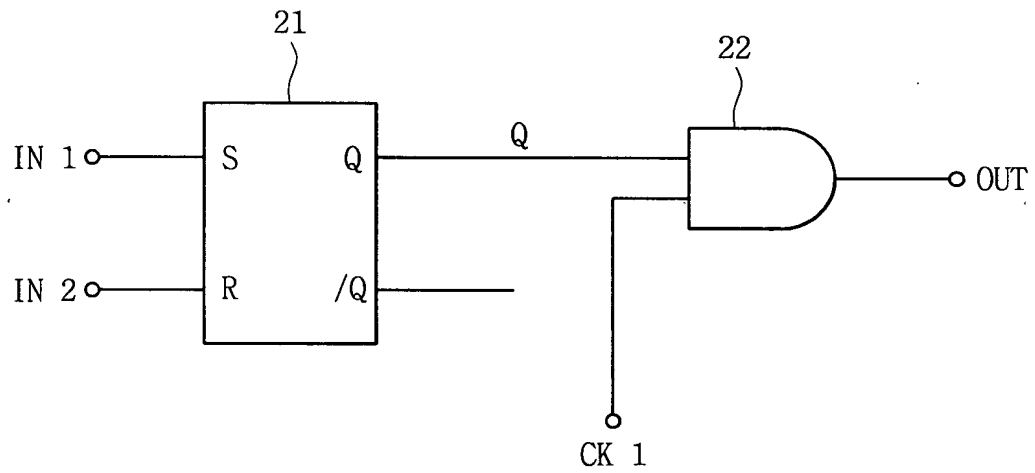


FIG. 3B
(PRIOR ART)

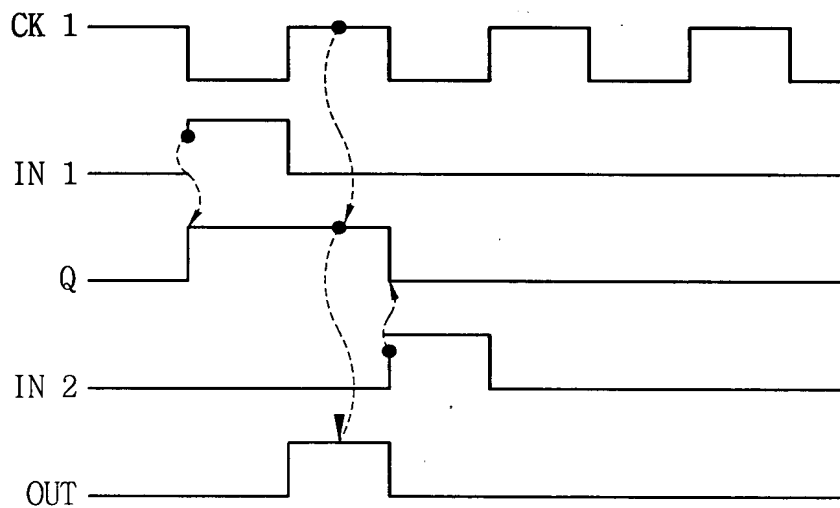


FIG. 3C
(PRIOR ART)

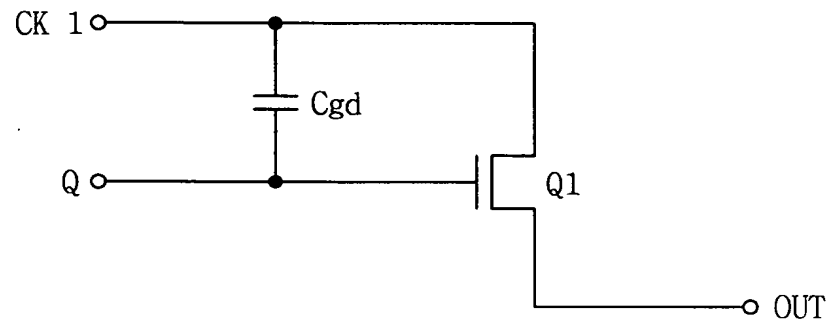


FIG. 4

200

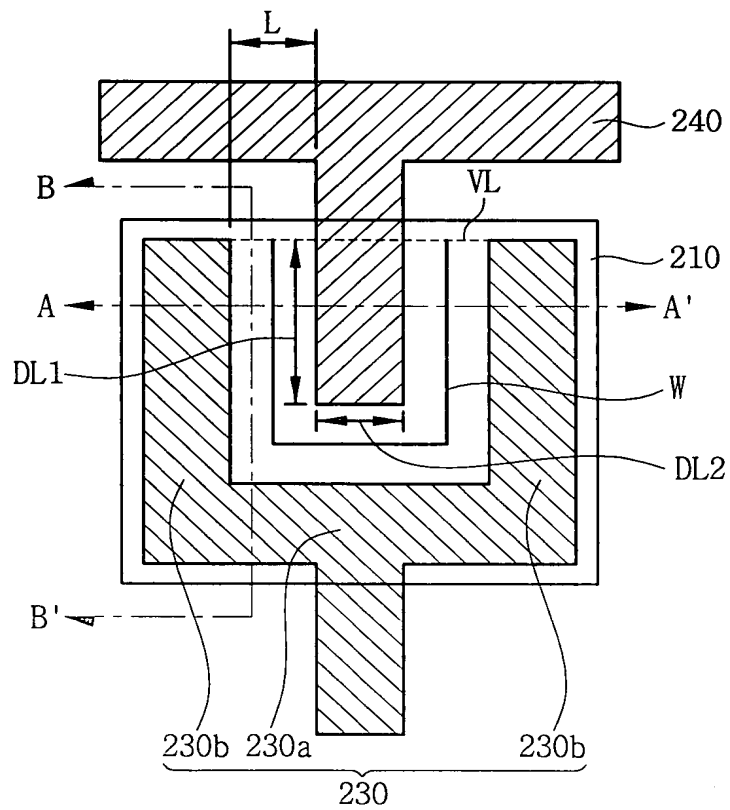


FIG. 5A

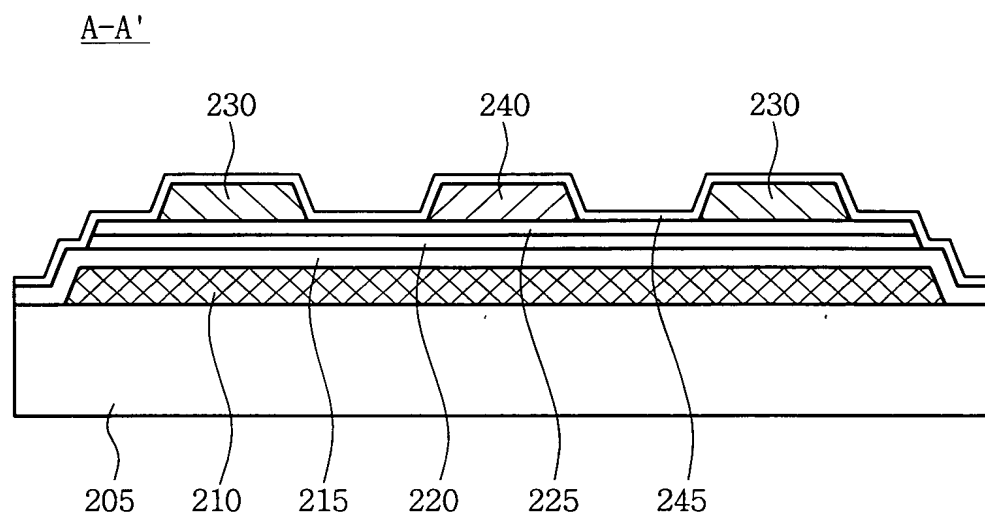


FIG. 5B

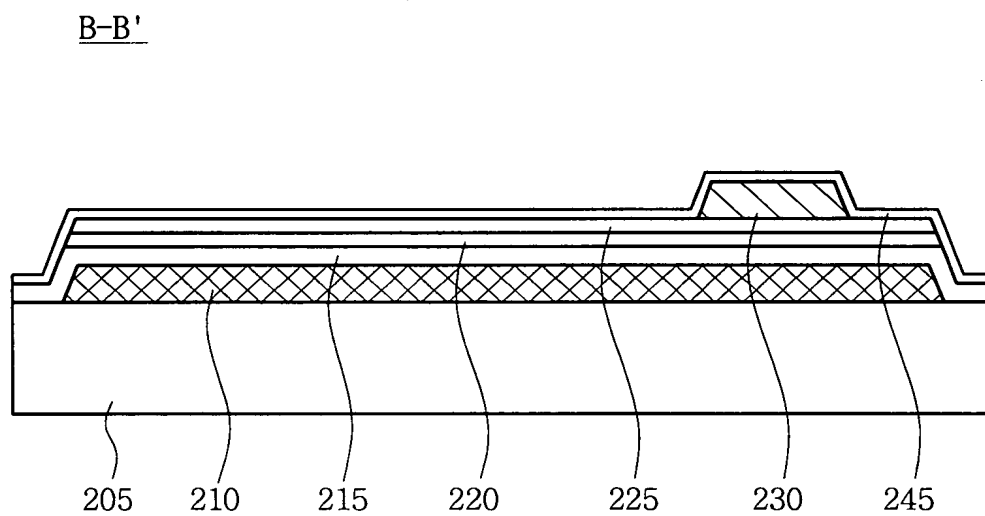


FIG. 6 is a cross-sectional view of a semiconductor device. The device includes a substrate 310 with a top layer 354a and a bottom layer 354b. A central region 111 contains a periodic array of gates 330, which are formed by a gate stack 336 on a gate dielectric 332. The gates are separated by spacers 334. The device is connected to a DRAIN on the left and a SOURCE on the right. Dimensions L and W are indicated. Cross-sections D-D', E-E', and C-C' are shown.

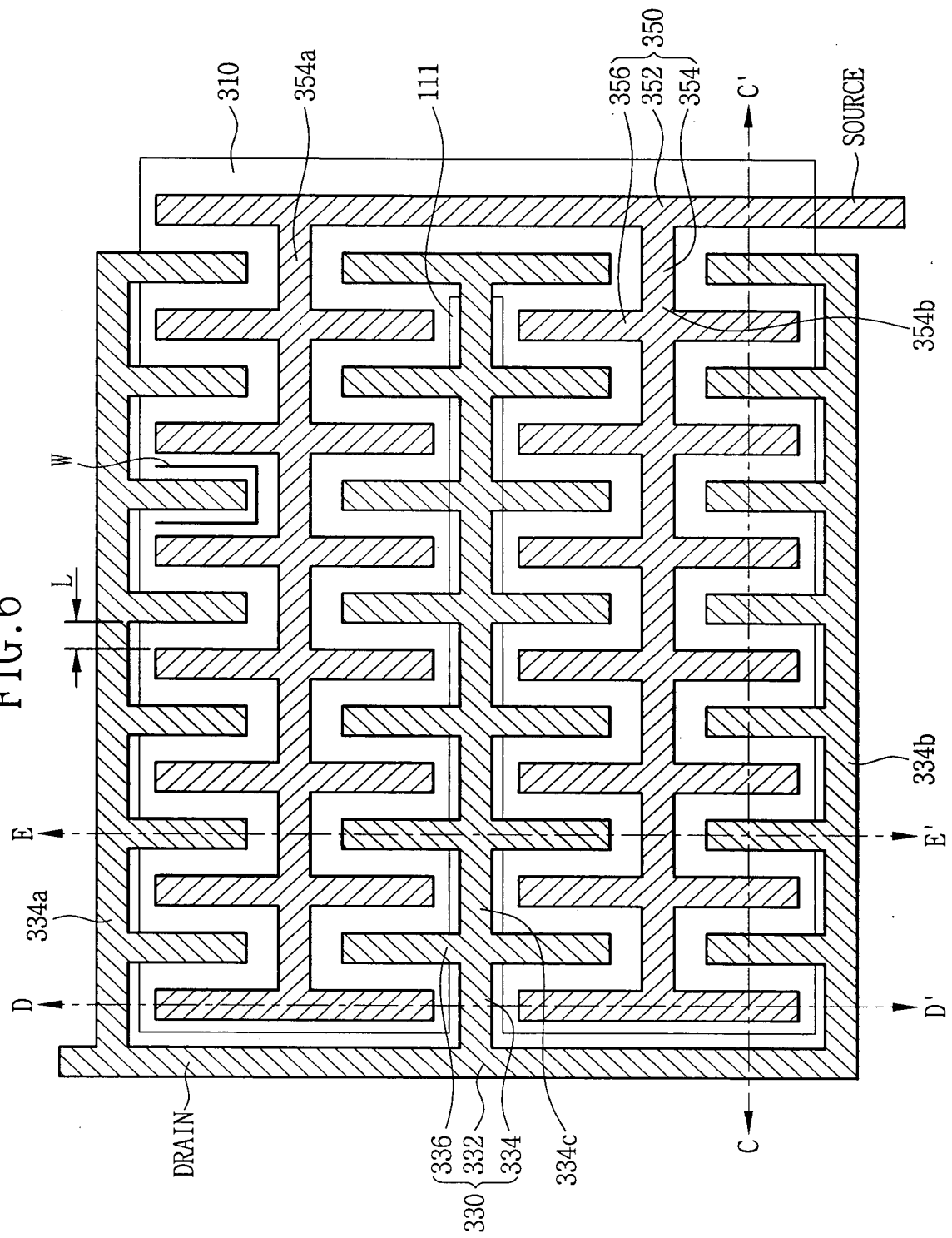


FIG. 7A

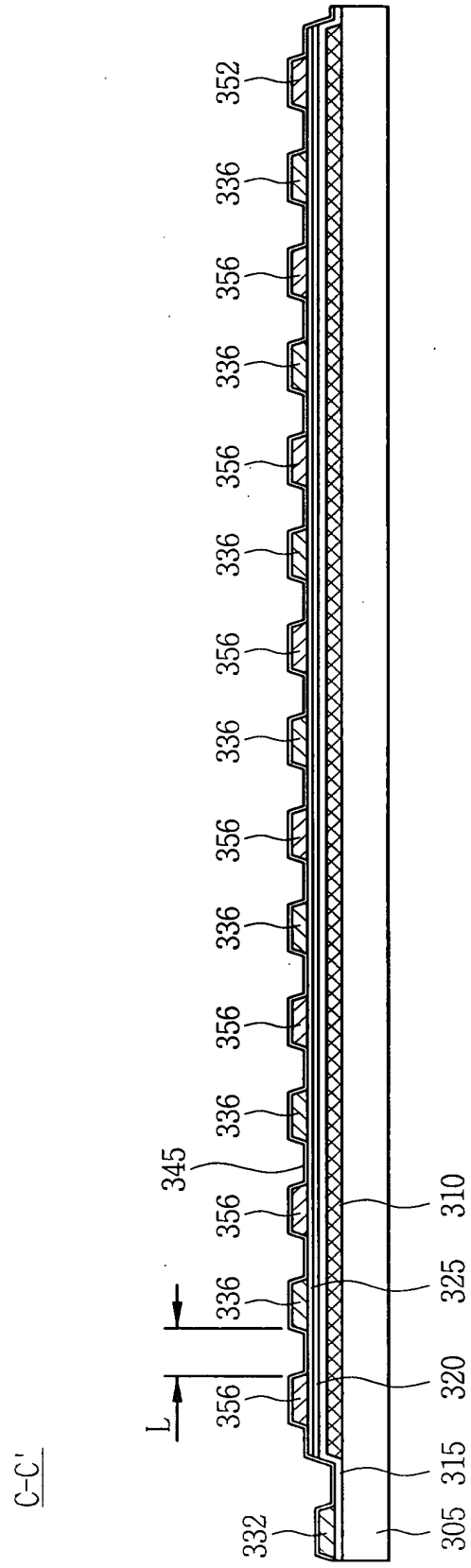


FIG. 7B

D-D'

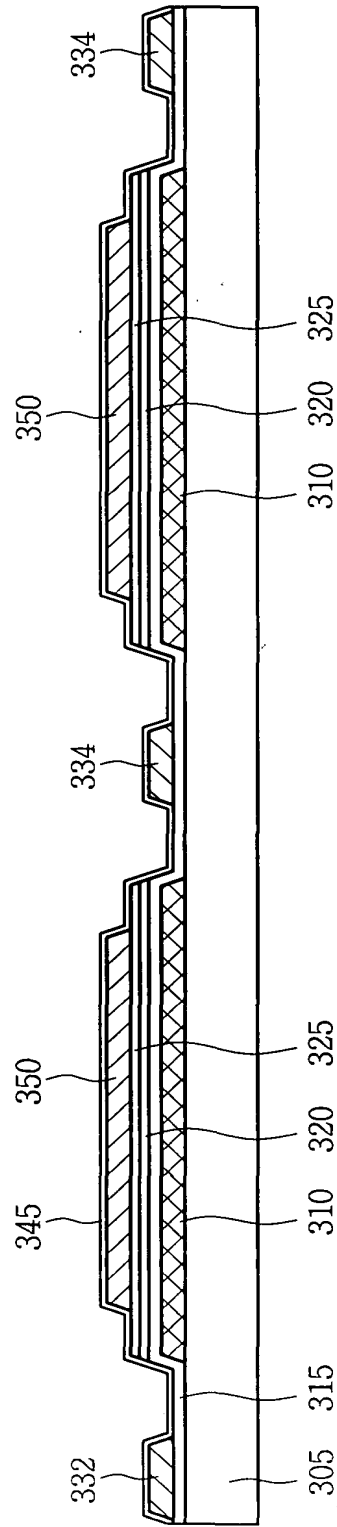


FIG. 7C

E-E'

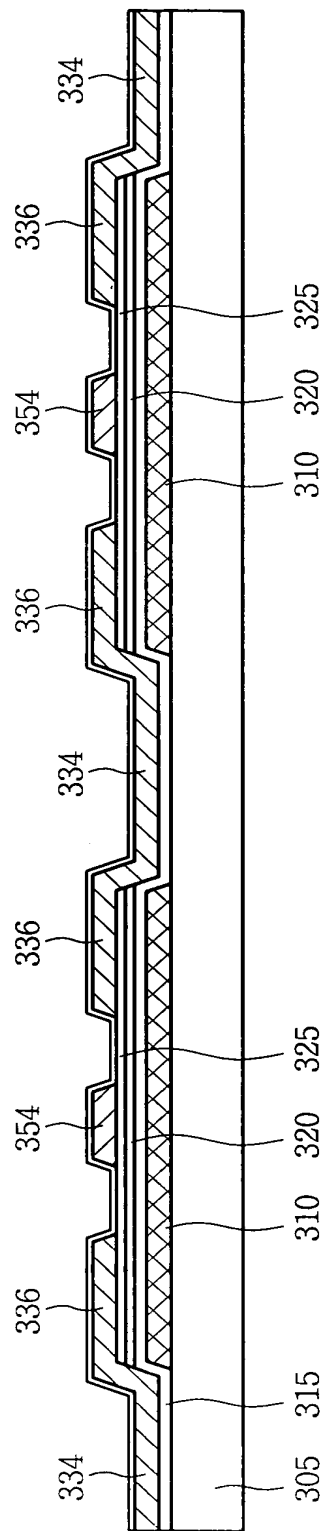


FIG. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 410. A top layer 430 is formed on the substrate 410. The top layer 430 contains a grid of rectangular openings 434a, 434b, 434c, and 434d. The openings are defined by a material 436. The top surface of the substrate is 454a, and the bottom surface is 454b. The side walls of the openings are 454c. The top layer 430 is bounded by a layer 450. The width of the openings is labeled L, and the width of the top layer is labeled W.

FIG. 9

